Integrated Millimeter-Wave Frequency Synthesizer based on Low-Power and Low-Noise Sub-Sampling Phase-Locked Loop

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Outline

- Apps & Pros of On-Chip mmWave Signal Generation
- Existing Topologies for Frequency Synthesis
- Low-Power & Low-Noise mmWave SSPLL
  - Proposed Dividerless Frequency Acquisition for SSPLL
  - Prototype 8.8mW 40.5GHz SSPLL
- Charge Pump Current Mismatch Compensation for SSPLL
  - Proposed compensation technique for SSPLL
  - Prototype SSPLL with CP compensation
- Conclusion
Applications of On-Chip mmWave Signal Generation

5G/6G Comm, Radar, Internet Of Things, Chemical Sensor, Heart-beat & Respiration Sensing

SatCom, Atomic Clock Excitation, Imaging, Biomedical

Favored Specifications:
• Low Power Consumption
• Low Noise (Pure Signal)
Pros of On-Chip mmWave SigGen

**Mini Hg Ion Clock**
- 4cm x 4cm x 4cm
- (40GHz mmW IC: 10mW)

**Displacement & Vibration Sensing**
- Laser Vibrometer
  - Resolution: 25nm
  - Power: 4W
  - Price: $4000

- 200GHz FMCW
  - Resolution: 54um
  - Power: 68mW

**Biomedical Sensing**
- Label-Free Detection
- Antigen-Antibody Reaction
- Evaluation of Micro-Organisms

**60/120GHz Dielectric Sensor**
- (40GHz mmW IC: 10mW)
- (mmW IC: 35mW)

**Discrete mmW SigGen:** 200mW

[Hoang, JPL & DARPA, IFCS 2021]

[Displacement & Vibration Sensing]

[Naghavi, ISSCC 2021]

[Mitsunaka, JSSC 2016]
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Background: PLL & SSPLL

Phase-Locked Loop (PLL)

Sub-Sampling PLL (SSPLL)

Frequency-acquisition is a must.
Existing Topologies for Frequency Synthesis

**Traditional PLL:**
- High phase noise (PN)
- mmWave ILFD needed:
  - High power
  - Limited locking range
  - Requires injecting power

**Traditional SSPLL:**
- Low in-band PN
- $f_{out}$ could be any $N \times f_{ref}$, always-on FLL is a must:
  - mmWave ILFD needed
  - High power

**Cascaded PLL/SSPLL:**
- Moderate power
- No FLL or ILFD, with IF > VCO2’s tuning range
- Added noise from 1st stage
- Constrained IF for low PN

**ILFM-based Synthesizers:**
- Low PN
- High power
- Limited locking range
- Requires injecting power

**Reference-Sampling PLL:**
- Not eligible for mmWave
- Need digital rectifier
- Type-I structure (no CP) is necessary for low PN

[Images of different topologies are shown, each with its own set of characteristics and references.]

References:
- K. O CICC ’06
- Szortyka ISSCC ’14
- El-Halwagy RFIC ’16
- A. Li JSSC ’14
- Sharma ISSCC ’18
- UC Davis
Motivation

How to achieve both low-noise & low-power?

A solution: Invent low-power freq-acquisition for SSPLL
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Proposed Dividerless Freq Acquisition for SSPLL

Dividerless Freq Acquisition (FA)
- Low-power, moderate-noise IF-PLL cascaded to SSPLL for FA
- mmWave ILFD avoided

Low PN mmWave Output
- After FA, SSPLL generates low-noise output with crystal reference

Sub-Sampling Lock Detector (SSLD)
- Automatic lock-status detection and reference switching for FA
- Low-power circuitry

Prototype Design: $f_{ref}=100\text{MHz}$, $IF=900\text{MHz}$, $f_{out}=40.5\text{GHz}$
Prototype 40.5GHz SSPLL with Dividerless FA

Total: 8.8mW

[Wang & Momeni TMTT '21]
Proposed SSLD: Analog Interface

Sampling SSPLL output with IF:

- SSPLL VCO TR designed with **only one** IF harmonic in each bank
- Sampled SSPLL output reflects:
  - $f_{out} = 40.5\text{GHz}$: $f_{det} \approx 0$
  - $f_{out} \neq 40.5\text{GHz}$: $f_{det} \geq f_{ref}$
- Low power in steady state

![Diagram showing sampling of SSPLL output with IF](image)
Proposed SSLD: Digital Logic

Lock Status Detection & FA Procedure

- SSPLL \( f_{\text{fout}} \neq 40.5\text{GHz} \): \( f_{\text{det}} \geq f_{\text{ref}} \)
- Set a threshold: \( 0 < f_{\text{th}} < f_{\text{ref}} \)
- Evaluate \( f_{\text{det}} \):
  - D-flip-flop as frequency counter
  - Count \( f_{\text{det}} \) within a time window
- If \( f_{\text{det}} > f_{\text{th}} \), go through FA procedure
  - \( \text{FA}_{\text{EN}}=1 \) to switch IF to SSPLL for FA(S2)
  - \( \text{FA}_{\text{EN}}=0 \) to switch \( f_{\text{ref}} \) back to SSPLL (S3)
  - \( \text{DET}_{\text{EN}}=1 \) to enable lock detection after loop settles (S1)

Prototype Design: \( f_{\text{ref}}=100\text{MHz}, \text{IF}=900\text{MHz}, f_{\text{th}}=40\text{MHz} \)
Different Loop Configurations for Two References

Different Loop Gains & BWs for the Two References

- For **IF**: high gain/BW for fast FA
- For **fref**: Noise-optimized gain/BW
- Gain changed in CP output current
- BW changed by varying LF resistor
- Consider the time sequence in switching
mmWave VCO & Buffers

- VCO TR designed smaller than IF in each bank
- Middle Buffer for better isolation. Two Output Buffers for SSPLL and SSLD, respectively

Measured VCO Tuning Range with Temperature Variation
Measurements: Frequency Spectrum

- **65nm** CMOS process
- Core area **0.6 mm²**
**Measurements: Phase Noise**

- **PN:** \(-96.6\) dBc/Hz @1MHz, \(-106.9\) dBc/Hz @10MHz
- **Jitter\(_{\text{rms}}\) (10kHz to 100MHz): 228 fs**
- In comparison: significant added noise from IF-PLL

**Room Temperature**

- **100MHz Ref. (sim)**
- **40.5GHz w/ 100MHz ref. (sim)**

**Robust Temperature Tolerance**

- **-40°C:** \(-94.6/-111.7\) dBc/Hz @1/10 MHz, Jitter\(_{\text{rms}}\)=235 fs
- **85°C:** \(-96.7/-105.1\) dBc/Hz @1/10MHz, Jitter\(_{\text{rms}}\)=232 fs

**Good Temperature-Variation Tolerance**

- **-40°C:** -94.6/-111.7 dBc/Hz @1/10 MHz, Jitter\(_{\text{rms}}\)=235 fs
- **85°C:** -96.7/-105.1 dBc/Hz @1/10MHz, Jitter\(_{\text{rms}}\)=232 fs
Measurements: Freq-Acquisition & Ref. Switching

Automatic Lock-Detection & Relock Procedure

- Force a wrong $f_{out}$, then close the loop and observe the operation of SSLD
- SSLD detects the wrong status and **relocks** the SSPLL to 40.5GHz
- **1us fast FA** with the high-BW loop
- $f_{out}$ deviation after ref. switching ($\Delta f_{out}=20MHz$) satisfies requirement
## Performance Comparison

<table>
<thead>
<tr>
<th>Topology</th>
<th>Tech (nm)</th>
<th>f&lt;sub&gt;ref&lt;/sub&gt; (MHz)</th>
<th>f&lt;sub&gt;out&lt;/sub&gt; (GHz)</th>
<th>TR (%)</th>
<th>PN&lt;sup&gt;a&lt;/sup&gt; (dBc/Hz)</th>
<th>Ref. Spur (dBc)</th>
<th>σ&lt;sub&gt;rms&lt;/sub&gt; (fs)</th>
<th>P&lt;sub&gt;DC&lt;/sub&gt; (mW)</th>
<th>Area (mm&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>FOM&lt;sub&gt;b&lt;/sub&gt;</th>
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<td>PLL+SSPLL</td>
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<td>SSPLL + SS LD</td>
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<td>100</td>
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<sup>a</sup> Normalized to 40.5GHz  
<sup>b</sup> FOM<sub>1</sub>=20 log(jitter/1s) + 10 log(P<sub>DC</sub>/1mW)  
<sup>c</sup> FOM<sub>2</sub>=20 log(jitter/1s) + 10 log(P<sub>DC</sub>/1mW) + 10 log(f<sub>ref</sub>/f<sub>out</sub>)
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Motive: CP Current Mismatch due to CLM

- Channel-length modulation (CLM) dominantly determines CP current mismatch.
- CLM is a function of $V_{ctrl}$.
- With high-freq references, CLM is even worse for the high-BW CP with short-channel devices.
- Exclusive to SSPLL:
  - CP currents vary with sampled input $V_{sam}$, unlike the constant-biased currents in PFD/CP PLL.
  - Existing compensation for PFD/CP PLL not eligible.
Motive: Effects of CP Current Mismatch on SSPLL

**Exclusive Effect for SSPLL**
- SSPD gain degeneration

**Other Effects**
- CP gain distortion
- Limited Vctrl locking range (LR)
  - Vctrl cannot further increase/decrease
  - More frequency overlap between adjacent VCO banks
  - More VCO banks to cover the total TR: more RF loss

[Wang & Momeni CICC '21]
Traditional PLL CP Current Mismatch Compensation

Traditional PLL CP currents are constant:

I_{up} = I_{dn}

How to compensate?

Sub-Sampling PLL

SSPLL CP currents vary with input (CP is gm):

I_{up} ≠ I_{dn}

How to compensate?
Proposed CP Mismatch Compensation for SSPLL

**Compensation Feedback**
- Dummy CP with **identical** sizing of CP to copy the current mismatch
- Compensation FB forces $V_{ctrl,dum}$ to track $V_{ctrl}$
- Identical compensation currents, $I_{comp}$ and $I_{comp,dum}$, for CP and CP$_{dum}$
- With any $V_{ctrl}$ value, since $I_{out,dum}=0$, $I_{out}$ is also 0 when CP input is $V_{sam}=0$. **Mismatch is cancelled.**
- FB **doesn’t prevent** $V_{sam}$ from changing $V_{ctrl}$

**Design Considerations**
- Design and layout matching for CP and CP$_{dum}$
- Enough BW for **timely** compensation
- Miller compensation to ensure **stability**

[Wang & Momeni TCAS-II ’21]
Simulated Compensation Result

Mismatch Compensation
- Simulate mismatch vs $V_{\text{ctrl}}$ with CP input $V_{\text{sam}}=0$
- Uncompensated CP mismatch: -50% to +70%
- Compensated CP mismatch: -5% to +14%

Transient Simulation
- During FA, $V_{\text{ctrl,dum}}$ tracks $V_{\text{ctrl}}$ timely
- Compensation FB loop is stable
Prototype 40.5GHz SSPLL with CP Compensation

Total: 9.5mW

Compensation: 0.36mW

100MHz Crystal

IF-PLL

x9

900MHz

Frequency

Acquisition

100MHz

Reference

SSPD

Compensated CP

Mismatch

Comp.

40.5GHz

VCO

Varactor

Banks

Output Buffer

Buffer

Gm

Digital Logic

Timer & State Machine

Sub-Sampling Lock Detector (SSLD)

fout 40.5GHz

40.5GHz

Decoupling Caps

VCO

Mid- Buf

Inj- Buf

SSPLL

(SSPD, Comp CP, LPF)

65nm CMOS, core area 0.6mm²

[Wang & Momeni TCAS-II ’21]
Measurements: Vctrl Locking Range

- Measure **locked Vctrl range** to evaluate the mismatch compensation result.
- Define an FOM to evaluate the **efficiency** in utilizing available CP supply voltage:
  \[
  \eta_{V_{ctrl}} = \frac{\text{Total TR (Hz)}}{\text{Total VCO bank number} \times V_{DD,CP} (V)}
  \]
- To cover the 10% TR:
  - **Uncompensated** CP needs 10 banks: \( \eta_{V_{ctrl}} = 50\% \)
  - **Compensated** CP needs 7 banks, \( \eta_{V_{ctrl}} = 72\% \)
- Improves bank efficiency: **Lower loss**
Measurements: Phase Noise & Jitter

- In-band PN is dominated by reference, CP compensation added noise is minute.
- No CP comp: -100.0/-105.9 dBc/Hz@1/10MHz, Jitter=204fs
- With CP comp: -100.5/-105.9 dBc/Hz@1/10MHz, Jitter=192fs

- With CP compensation, SSPLL Vctrl locking range is extended, and SSPD gain distortion is alleviated.
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$^d$ Calculated with $2V_{DD,CP}$ due to the differential $V_{ctrl}$
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Conclusion

• On-chip mmWave SSPLL:
  • Low power consumption & low noise;
  • Promising candidate for **IoT sensors**: displacement/vibration, chemical, atomic clock etc.

• A **dividerless frequency acquisition** structure is proposed to achieve sub-10mW record low power consumption in a 40.5GHz SSPLL.

• A low-power **charge pump current mismatch compensation** method for SSPLL is proposed to increase supply voltage utility efficiency by 50%.

• Proposed techniques enhance SSPLL’s eligibility in **power-stringent** applications, especially for IoT sensors design.
Thank you!
References


